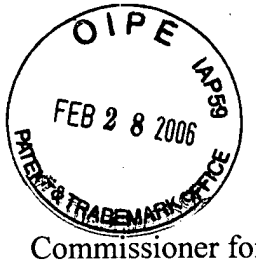
IME 03-009



Application No.10/767,275

IFW/AF

TO: Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

FROM: George O. Saile, Reg. No. 19,572
28 Davis Ave.
Poughkeepsie, N. Y. 12603

SUBJECT:

Serial #:	10/767.275
File Date:	01/29/04
Inventors:	Ming Fu Li
Examiner:	Nadav, Ori.
Art Unit:	2811
Title:	CMOS Compatible Low Band Offset Double Barrier Resonant Tunneling Diode

RESPONSE TO OFFICE ACTION

In response to the Office Action of 01/05/06 please amend the above identified application for patent as follows:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents P. O. Box 1450, Alexandria, VA 22313-1450 on February 23, 2006.

Signature _____ Date: 2/23/06
Stephen B. Ackerman, Reg. No. 37,761

Amendments to the Claims are reflected in the listing of claims that begins on page 3 of this paper.

Remarks/Arguments begin on page 6 of this paper.